

	L #	Hits	Search Text	DBs
1	L3	44	(reorder\$3 order\$3) near99 mask\$3 near99 (swap\$4 centrifug\$3)	USPAT; US-PGPUB

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FIG. 76A

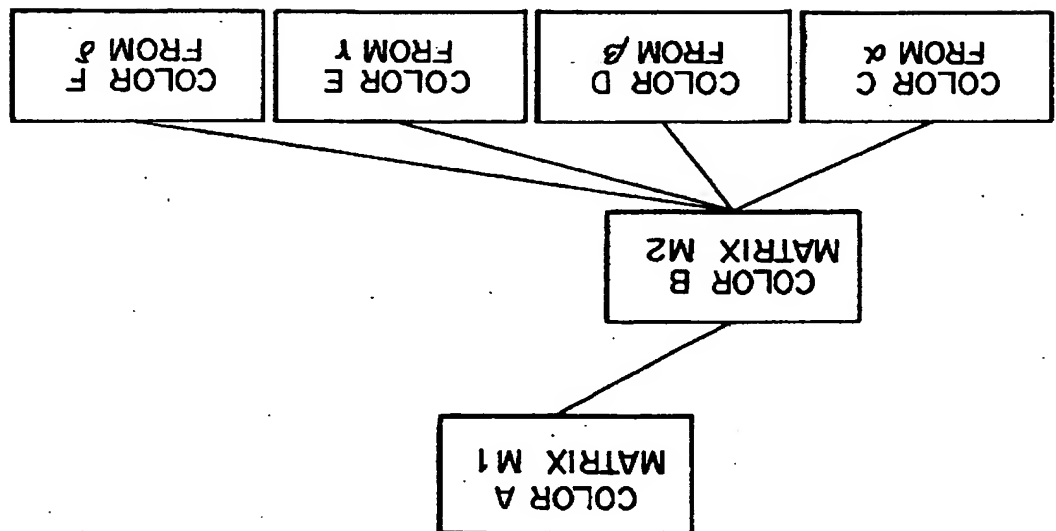
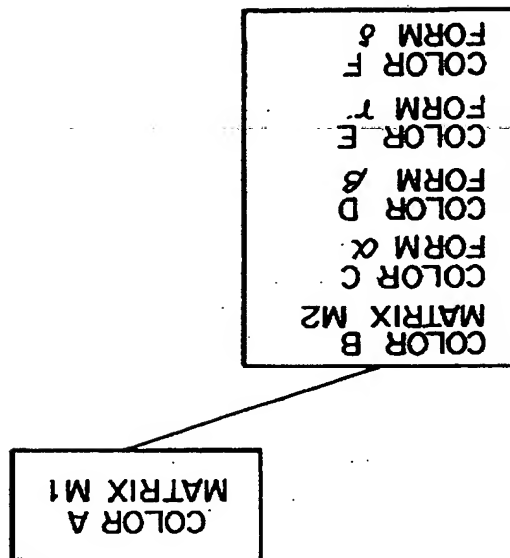


FIG. 76B



	Docum ent ID	U	Title	Current OR
1	US 20030 20724 7 A1	<input type="checkbox"/>	Preparation of red blood cells having reduced immunogenicity	435/2
2	US 20020 16980 8 A1	<input type="checkbox"/>	System and method for reordering data	708/204
3	US 20020 13143 2 A1	<input type="checkbox"/>	Method and apparatus for ternary content addressable memory (TCAM) table management	370/408
4	US 20020 05521 9 A1	<input type="checkbox"/>	Swapped drain structures for electrostatic discharge protection	438/231
5	US 66836 15 B1	<input type="checkbox"/>	Doubly-virtualized texture memory	345/543
6	US 66779 52 B1	<input type="checkbox"/>	Texture download DMA controller synching multiple independently-running rasterizers	345/505
7	US 66503 33 B1	<input type="checkbox"/>	Multi-pool texture memory management	345/552
8	US 66188 04 B1	<input type="checkbox"/>	System and method for rearranging bits of a data word in accordance with a mask using sorting	712/300
9	US 65873 22 B2	<input type="checkbox"/>	Swapped drain structures for electrostatic discharge protection	361/56
10	US 65871 13 B1	<input type="checkbox"/>	Texture caching with change of update rules at line end	345/557
11	US 63593 14 B1	<input type="checkbox"/>	Swapped drain structures for electrostatic discharge protection	257/355
12	US 62970 82 B1	<input type="checkbox"/>	Method of fabricating a MOS transistor with local channel ion implantation regions	438/217
13	US 61768 62 B1	<input type="checkbox"/>	Hair-removing device with rotary roller equipped with pain-soothing device	606/133
14	US 61191 98 A	<input type="checkbox"/>	Recursive address centrifuge for distributed memory massively parallel processing systems	711/5
15	US 60947 15 A	<input type="checkbox"/>	SIMD/MIMD processing synchronization	712/20
16	US 59665 28 A	<input type="checkbox"/>	SIMD/MIMD array processor with vector processing	712/222
17	US 59637 46 A	<input type="checkbox"/>	Fully distributed processing memory element	712/20
18	US 59637 45 A	<input type="checkbox"/>	APAP I/O programmable router	712/13
19	US 58782 41 A	<input type="checkbox"/>	Partitioning of processing elements in a SIMD/MIMD array processor	712/203
20	US 58706 19 A	<input type="checkbox"/>	Array processor with asynchronous availability of a next SIMD instruction	712/20
21	US 58571 09 A	<input type="checkbox"/>	Programmable logic device for real time video processing	712/37

FIG. 77A

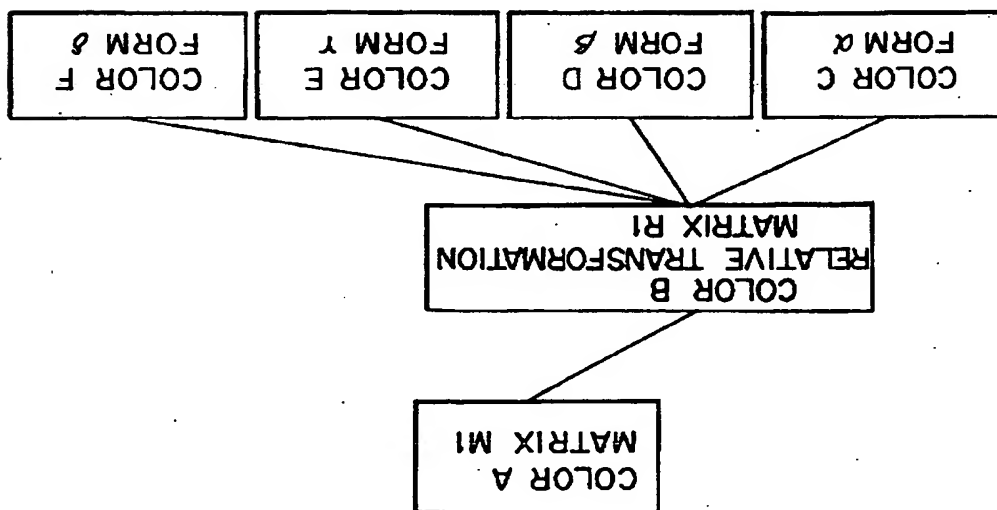
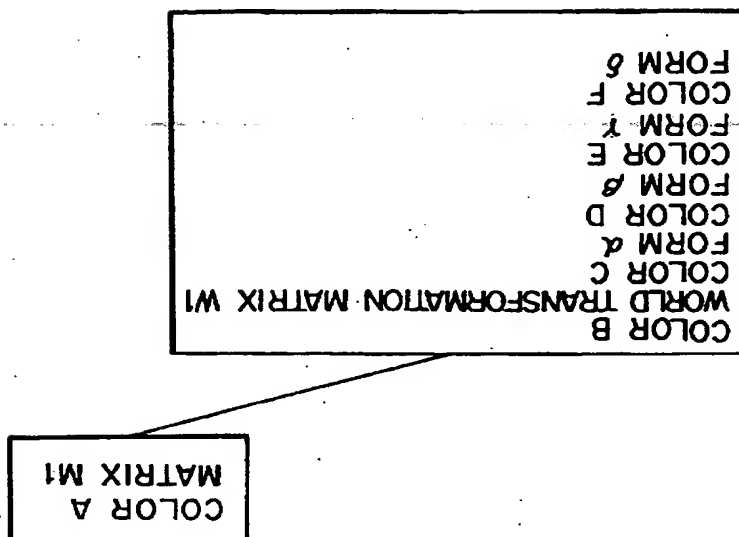


FIG. 77B



	Docum ent ID	U	Title	Current OR
22	US 58420 31 A	<input type="checkbox"/>	Advanced parallel array processor (APAP)	712/23
23	US 57940 59 A	<input type="checkbox"/>	N-dimensional modified hypercube	712/10
24	US 57651 81 A	<input type="checkbox"/>	System and method of addressing distributed memory within a massively parallel processing system	711/5
25	US 57650 11 A	<input type="checkbox"/>	Parallel processing system having a synchronous SIMD processing with processing elements emulating SIMD operation using individual instruction streams	712/20
26	US 57615 23 A	<input type="checkbox"/>	Parallel processing system having asynchronous SIMD processing and data parallel coding	712/20
27	US 57548 71 A	<input type="checkbox"/>	Parallel processing system having asynchronous SIMD processing	712/20
28	US 57520 67 A	<input type="checkbox"/>	Fully scalable parallel processing system having asynchronous SIMD processing	712/16
29	US 57349 21 A	<input type="checkbox"/>	Advanced parallel array processor computer package	712/10
30	US 57179 44 A	<input type="checkbox"/>	Autonomous SIMD/MIMD processor memory elements	712/20
31	US 57179 43 A	<input type="checkbox"/>	Advanced parallel array processor (APAP)	712/20
32	US 57130 37 A	<input type="checkbox"/>	Slide bus communication functions for SIMD/MIMD array processor	702/33
33	US 57109 35 A	<input type="checkbox"/>	Advanced parallel array processor (APAP)	712/20
34	US 57088 36 A	<input type="checkbox"/>	SIMD/MIMD inter-processor communication	712/20
35	US 56969 22 A	<input type="checkbox"/>	Recursive address centrifuge for distributed memory massively parallel processing systems	711/5
36	US 56258 36 A	<input type="checkbox"/>	SIMD/MIMD processing memory element (PME)	709/214
37	US 55903 45 A	<input type="checkbox"/>	Advanced parallel array processor (APAP)	712/11
38	US 55881 52 A	<input type="checkbox"/>	Advanced parallel processor including advanced support hardware	712/16
39	US 54974 98 A	<input type="checkbox"/>	Video processing module using a second programmable logic device which reconfigures a first programmable logic device for data transformation	710/104
40	US 49673 36 A	<input type="checkbox"/>	High voltage bridge interface	363/132
41	US 43777 31 A	<input type="checkbox"/>	Device for automatically interrupting the supply of electric power to a motor and its utilization	200/80R
42	US 42714 69 A	<input type="checkbox"/>	Method for detecting knocking in internal combustion engine	701/111
43	US 36838 77 A	<input type="checkbox"/>	FUEL FEED DEVICES FOR INTERNAL COMBUSTION ENGINES	123/477
44	US 36173 39 A	<input type="checkbox"/>	SPRAY COATING METHODS	427/240

POINTER TO PARENT NODE			
COLOR INFORMATION (NOT EXISTING IF ATTRIBUTE IS INHERITED FROM PARENT)			
TEXTURE INFORMATION (NOT EXISTING IF ATTRIBUTE IS INHERITED FROM PARENT)			
MATRIX INFORMATION (NOT EXISTING IF ATTRIBUTE IS INHERITED FROM PARENT)			
NUMBER OF CHILDREN	POINTER TO CHILD NODE	POINTER TO CHILD NODE	---

FIG. 78

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